Docket No.: M4065.0067/P067
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:
Warren M. Farnworth

Application No.: 09/118,080 Art Unit: 2827

Filed: July 17, 1998 (RCE) Examiner: A. Chambliss

For: LEAD OVER CHIP SEMICONDUCTOR DEVICES WITH A BALL GRID ARRAY

APPELLANT'S BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an appeal pursuant to 35 U.S.C. § 134(a) and 37 C.F.R. §§ 1.191 et seq., from the final rejection of claims 1-7, 10-18 and 31-33 (all of the rejected claims) of the above-identified application. This Brief is being submitted in triplicate. An appendix of claims is attached, and the applicable fee ($330.00; 37 C.F.R. § 1.17(c)) is also attached. Please charge any deficiency in the fees associated with this paper to Deposit Account No. 04-1073. The Notice of Appeal was filed on April 19, 2004.

06/23/2004 CNGUYEN 00000120 09118080
01 FC:1402 330.00 OP

I. Real Party in Interest

The real party in interest in this appeal is Micron Technology, Inc. (the assignee of the application).

II. Related Appeals and Interferences

There are no appeals or interferences known to Appellant, his legal representative, or the assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. Status of Claims

Claims 1-7 and 10-33 are pending in the application. Claims 8 and 9 are canceled. Claims 1, 2, 4-7, 10-14 and 16-18 are finally rejected under 35 U.S.C. § 103 as being unpatentable over Heo in view of Master Bond Polymer System EP31. Claims 3 and 15 are rejected under § 103 as being unpatentable over Heo in view of the Master Bond document and further in view of Chang. Claims 19-30 are withdrawn from further consideration, and are not involved in this appeal. Claims 31-33 are rejected under § 103 as being unpatentable over Heo in view of Akagawa. As noted above, this is an appeal from the rejection of claims 1-7, 10-18 and 31-33.

IV. Status of Amendments

There has been no amendment subsequent to the February 13, 2004 final Office Action. A Request for Reconsideration was filed on March 29, 2004. An Advisory Action was mailed on April 5, 2004.

V. Summary of Invention

Claim 1 relates to a device that has a semiconductor chip 14 and a single dielectric layer 22 (Fig. 2). There are electrically conductive leads 24-30 on the dielectric layer 22, and an adhesive material 20 is located between the chip 14 and the layer 22. The adhesive material 20 is a low temperature curing material – one that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit – such that misalignment between the chip 14 and the dielectric layer 22 can be avoided (specification, page 10, lines 10 and 11).[1]

According to a preferred embodiment of the invention, the dielectric layer 22 includes polyimide or benzocylobutene (page 9, lines 10+), or it may include a metal alloy and a polymer coating.

[1] Although specific references to the drawings and specification are provided herein for illustrative/exemplary purposes pursuant to 37 C.F.R. § 1.192(c)(5), the claimed invention should not be limited to the preferred embodiments. The claimed invention is defined in the respective claims.

According to another aspect of the invention, bond wires 36, 38 (Fig. 3) connect the semiconductor chip 14, 16 to electrically conductive leads 24-30. The wires 36, 38 may be encapsulated in resin material 40 (Fig. 4). An opening 18 (Fig. 2) may be defined in the dielectric layer 22, and the wires 36, 38 and the resin material 40 (which may be a glob top encapsulant) may be located in the opening 18. Plural openings 18 may be slot-shaped and punched through the layer 22 to expose aligned bond pads 16. A ball grid array 50-56 may be provided on the leads 24-30.

Further, the claimed invention relates to a taped (12) semiconductor product (Figs. 1 and 2) with openings 18 aligned with integrated circuits 16. According to this aspect of the invention, the tape 12 includes a single dielectric layer 22 and electrically conductive leads 24-30, the leads 24-30 being printed on the layer 22. Wires 36-38 extend through the openings 18 and are electrically connected to the circuits 16. Adhesive material 20 is located between the tape 12 and the circuits 16. According to this aspect of the invention, the adhesive material 20 is one that cures to about ninety percent of its maximum strength within twenty four to thirty six hours at room temperature, so as to avoid misalignment between the tape 12 and the integrated circuits 16.

According to yet another aspect of the invention, via holes 80 (Fig. 8) may defined in the single dielectric layer 82, and metal may be located in the via holes 80, connected (26, 28) to the leads 24, 30. According to this aspect of the invention, the ball grid array 50-56 can be located within the periphery 62 of the chip 76.

VI. Issues

A. Should the rejection of claims 1, 2, 4-7, 10-14 and 16-18 under 35 U.S.C. § 103 as being unpatentable over Heo in view of the Master Bond document be reversed?

B. Should the rejection of claims 3 and 15 under § 103 as being unpatentable over Heo in view of the Master Bond document and further in view of Chang be reversed?

C. Should the rejection of claims 31-33 under § 103 as being unpatentable over Heo in view of Akagawa be reversed?

VII. Grouping of Claims

The claims do not stand or fall together. The reasons why the claims are believed to be separately patentable are set forth below in the Argument section of this Brief.

VIII. Argument

Claims 1-7 each recite a "low temperature curing" adhesive material. According to the claims, the adhesive material is one that "cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit." The low temperature curing aspect of the recited adhesive material is an important feature of the claimed invention. Among other things, it "avoid[s]

misalignment between said chip and said single dielectric layer," as discussed in Appellant's specification.

Heo refers to a semiconductor package comprising a chip 11, an epoxy adhesive 30, and a non-conductive film 21. Heo fails to disclose or suggest an adhesive material that "cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit," and the Examiner does not contend otherwise. The Examiner contends it would have been obvious to substitute an adhesive mentioned in the Master Bond document for the Heo adhesive 30. The motivation for such substitution, according to the Examiner, would have been to provide "high peel strength and good adhesion" between the Heo chip 11 and film 21.

Appellant respectfully submits, however, that many structural adhesives could be said to have "high peel strength and good adhesion." To argue, as the Examiner does, that it would have been obvious to substitute the Master Bond adhesive for the Heo adhesive 30 because the Master Bond adhesive is a "good" adhesive, is simply another way of arguing that it would have been obvious to try all adhesives as possible substitutes for the Heo adhesive 30. It is well settled that such an obvious to try analysis does not lead to a proper prima facie case of obviousness.

In In re Fine, 837 F.2d 1071 (Fed. Cir. 1988), the PTO had a primary reference that disclosed a chromatograph, a combustion means, and a sulfur detector, and a secondary reference that taught a nitric oxide detector. According to the PTO, "substitution of one type of detector for another . . . would have been within the skill of the art." Id. at 1074; accord M.P.E.P. § 2143.01, page 2100-125. The U.S. Court of Appeals for the Federal

Circuit reversed the PTO and agreed with the applicant that such an "obvious to try" analysis was "unacceptable." 837 F.2d at 1074. In re Fine would not have been decided differently if the secondary reference had added that its detector was a "good" detector. Likewise, in the present case, the fact that the Master Bond adhesive is said to have "good" adhesive properties provides no sufficient reason under § 103 to substitute it for the Heo adhesive 30.

The Examiner has also noted that the Master Bond adhesive is said to be a "superb electrical insulator." This adds nothing in terms of motivation either, however, since there is nothing in the references, considered singly or together, to suggest that it would have been of any advantage to have a "superb electrical insulator" between the Heo chip 11 and film 21. The Heo film 21 was already non-conductive (Heo, column 5, line 48).

In sum, Heo fails to disclose the adhesive material of claims 1-7, as acknowledged by the Examiner, and there is no sufficient motivation for substituting the Master Bond adhesive for the Heo adhesive 30. Therefore, claims 1-7 should be allowable over Heo and the Master Bond document.

The Examiner has also argued, in effect, that the "low temperature curing" aspect of the adhesive material of claims 1-7 should be ignored. In response, Appellant respectfully submits that the "low temperature curing" limitation is like the structural limitations listed in M.P.E.P. § 2113, second paragraph ("intermixed," "ground in place," "etched," etc.). There are structural differences between devices that have the recited "low temperature curing" adhesive material and those that do not. The low temperature curing adhesive material limitation of claims 1-7 should not be ignored.

Claims 10-12 each recite adhesive material that "cures to about ninety percent of its maximum strength within twenty four to thirty six hours at room temperature." Claims 13-18 each recite adhesive material that is "capable of curing to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit so as to avoid misalignment." Claims 10-18 should be allowable for reasons similar to those given in connection with claim 1, and there are other reasons why the claims should be allowable.

Claims 31-33 are rejected under 35 U.S.C. § 103 as being unpatentable over Heo in view of Akagawa. Claims 31-33 each recite an anisotropically conductive adhesive material. The material is located between a dielectric layer and a chip. Heo fails to disclose or suggest the recited material. The Examiner contends it would have been obvious to substitute an anisotropically conductive adhesive material for the Heo adhesive 30. The motivation for such substitution, according to the Examiner, would have been to provide a "bonding material" between the chip 11 and film 21. Please note, however, that the Heo device already has a "bonding material" (the adhesive 30) between the chip 11 and film 21. Appellant respectfully submits that the rejection of claims 31-33 amounts to nothing more than an argument that it would have been obvious to try any and all materials that are "bonding materials" as a possible substitute for the Heo adhesive, which is not a proper basis for a § 103 rejection.

With respect to claims 31-33, the Examiner has also made an argument with respect to providing an "additional" source of electrical connection for the "semiconductor device." This argument is not understood, and the Examiner has not attempted to explain

it further. It is not understood which "semiconductor device" the Examiner is referring to, or why the adhesive would be considered an "additional" source of electrical connection.

The rejection of claims 1, 2, 4-7, 10-14 and 16-18 under 35 U.S.C. § 103 as being unpatentable over Heo in view of the Master Bond document, claims 3 and 15 under § 103 as being unpatentable over Heo in view of the Master Bond document and further in view of Chang, and claims 31-33 under § 103 as being unpatentable over Heo in view of Akagawa, should be reversed

Dated: June 21, 2004

Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 775-4742
Attorneys for Applicant

APPENDIX

1. A semiconductor device, comprising:

a semiconductor chip;

a single dielectric layer;

electrically conductive leads on said dielectric layer; and

a low temperature curing adhesive material that cures to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit so as to avoid misalignment between said chip and said single dielectric layer, said low temperature curing adhesive material being located between said semiconductor chip and said dielectric layer.

2. The semiconductor device of claim 1, wherein said single dielectric layer includes polyimide.

3. The semiconductor device of claim 1, wherein said single dielectric layer includes benzocylobutene.

4. The semiconductor device of claim 1, further comprising bond wires connecting said semiconductor chip to said electrically conductive leads.

5. The semiconductor device of claim 4, further comprising resin material encapsulating said bond wires.

6. The semiconductor device of claim 5, further comprising an opening defined in said single dielectric layer, and wherein said bond wires and said resin material are located in said opening.

7. The semiconductor device of claim 6, further comprising a ball grid array on said leads.

10. A taped semiconductor product, comprising:

integrated circuits formed in semiconductor material;

a tape having openings aligned with said integrated circuits, wherein said tape includes a single dielectric layer and electrically conductive leads, said leads being printed on said single dielectric layer;

bond wires extending through said openings, said bond wires being electrically connected to said integrated circuits; and

adhesive material between said tape and said integrated circuits, wherein said adhesive material cures to about ninety percent of its maximum strength within twenty four to thirty six hours at room temperature so as to avoid misalignment between said tape and said integrated circuits.

11. The taped semiconductor product of claim 10, further comprising glob top encapsulant material in said openings.

12. The taped semiconductor product of claim 11, further comprising a ball grid array for each of said integrated circuits, said ball grid arrays being located on said electrically conductive leads.

13. A tape for semiconductor devices, said tape comprising:

a single dielectric layer having openings;

electrically conductive leads associated with said openings, said leads being printed on said dielectric layer; and

a low temperature curing adhesive material located so as to provide adhesion between a semiconductor chip and said dielectric layer, said adhesive material capable of curing to about ninety percent of its maximum strength within two to three hours without exceeding one hundred fifty degrees Fahrenheit so as to avoid misalignment between said chip and said dielectric layer.

14. The tape of claim 13, wherein said single dielectric layer includes polyimide.

15. The tape of claim 13, wherein said single dielectric layer includes benzocylobutene.

16. The tape of claim 13, wherein said dielectric material includes a metal alloy and a polymer coating.

17. The tape of claim 13, wherein said openings are slot-shaped to expose aligned bond pads.

18. The tape of claim 17, wherein said openings are punched through said dielectric layer.

31. A semiconductor device, comprising:

a semiconductor chip;

a single dielectric layer;

electrically conductive leads on said single dielectric layer; and

an anisotropically conductive adhesive material located between said single dielectric layer and said semiconductor chip, said adhesive material capable of curing so as to avoid misalignment between said dielectric layer and said chip.

32. The semiconductor device of claim 31, further comprising via holes defined in said single dielectric layer, and metal located in said via holes, said metal being connected to said leads.

33. The semiconductor device of claim 32, further comprising a ball grid array on said leads, said ball grid array being located within the periphery of said chip.

PTO/SB/17 (10-03)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/118,080
Filing Date	July 17, 1998
First Named Inventor	Warren M. Farnworth
Examiner Name	A. Chambliss
Art Unit	2827
Attorney Docket No.	M4065.0067/P067

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☒ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 04-1073

Deposit Account Name: Dickstein Shapiro Morin & Oshinsky LLP

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	-20** =		x		=	
Independent Claims	-3** =		x		=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Mark J. Thronson	*Registration No. (Attorney/Agent)*	33,082	*Telephone*	(202) 775-4742
Signature				*Date*	June 21, 2004